Nov - Dec 2009

Total No. of Questions—12] [Total No. of Printed Pages—4+1

[3662]-211

S.E. (Information Technology) (First Sem.) EXAMINATION, 2009

COMPUTER ORGANIZATION

(2008 COURSE)

Time : Three Hours **Maximum Marks : 100**

N.B. :— (*i*) Answer *three* questions from Section I and *three* questions from Section II.

(*ii*) Answers to the two Sections should be written in separate answer books.

(*iii*) Neat diagrams must be drawn wherever necessary.

(*iv*) Figures to the right indicate full marks.

(*v*) Assume suitable data, if necessary.

SECTION I

1. (*a*) Draw flowchart of Booth's algorithm for signed multiplication and multiply the following signed 2's complement numbers. Justify your answer. [10]

Multiplicand = 110011, Multiplier = 101100

P.T.O.

(b) Compare IEEE standard single precision and double precision floating point formats. Represent $-(84.25)_{10}$ in single precision and double precision IEEE format. [8]

Or

2. (a) Write Booth's algorithm for restoring unsigned division and divide the following unsigned numbers and justify your answer. [10]

Dividend = 1000, Divisor = 11.

(b) Explain IAS (Von Neumann) architecture with the help of a neat diagram. [8]

3. (a) State design factors in design of instruction format. Draw instruction format for INTEL processors and explain various fields in it. [8]

(b) Draw and explain architecture of 8086. [8]

Or

4. (a) Draw timing diagram for memory read cycle of 8086 and list operations in each T state. [8]

(b) State and explain any 4 addressing modes with examples for INTEL processors. [8]

5. (*a*) Explain design of multiplier control unit using any hardwired control unit. [8]

(*b*) Draw and explain the micro-programmed control unit. [8]

Or

6. (*a*) Draw neat diagram of single bus organization of a CPU showing ALU, all types of registers and the data paths among them. Compare it with multiple bus organisation of CPU. [8]

(*b*) Compare :

(*i*) Hardwired and Micro-programmed control.

(*ii*) Horizontal and Vertical micro-instruction format. [8]

SECTION II

7. (*a*) What is virtual memory ? Explain address translation mechanism for converting virtual address into physical address with neat diagram. [10]

(*b*) What is cache coherence and discuss MESI protocol ? [8]

Or

8. (*a*) State cache mapping techniques. Draw and discuss them with their merits and demerits. [10]

(*b*) Write short notes on (any *two*) : [8]

(*i*) EEPROM

(*ii*) Magnetic disk

(*iii*) Optical disk

(*iv*) RAID.

9. (*a*) Explain the following : [8]

(*i*) Scanner

(*ii*) Keyboard.

(*b*) What is programmed I/O and interrupt driven I/O ? Compare them. [8]

Or

10. (*a*) What is DMA ? Explain DMA operation with a diagram. Also explain data transfer modes in DMA. [8]

(*b*) Explain the function and features of IC 8255 and 8251. [8]

11. (*a*) Draw and explain loosely coupled multiprocessor configuration with its merits. [8]

(*b*) Explain briefly :

(*i*) Instruction pipelining

(*ii*) Superscalar architecture. [8]

Or

12. (*a*) What is cluster ? State the advantages of clustering. Explain cluster classification. [8]

(*b*) Compare :

(*i*) UMA and NUMA

(*ii*) RISC and CISC. [8]