UNIVERSITY OF PUNE
[4362]-221
S. E. (Information Technology)
(Semester - I) Examination - 2009
COMPUTER ORGANIZATION
(2008 Pattern)

Total No. of Questions : 12 **[Total No. of Printed Pages :4]**
[Time : 3 Hours] **[Max. Marks : 100]**

Instructions

(1) Answer Q1 or Q2, Q3 OR Q4, Q5 OR Q6, From section I and Q7 OR Q8, Q9 OR Q10, Q11 OR Q12 From section II.
*(2) Answers to the **two sections** should be written in **separate answer-books**.*
(3) Neat diagrams must be drawn wherever necessary.
(4) Black figures to the right indicate full marks.
(5) Assume suitable data, if necessary.

SECTION-I

Q.1 (a) Compare Restoring and Non-Restoring division algorithm. Perform the division using restoring division algorithm.

Dividend =17; Divisor = 03 [10]

(b) Draw IEEE standards for Single precision and double Precision floating point Numbers. Represent $(309.1875)_{10}$ in single precision and double precision format. [8]

OR

Q.2 (a) Draw Flowchart of Booth's algorithm for non-restoring unsigned division and divide the following unsigned numbers and justify your answer. [10]

Dividend = 1011 ; Divisor = 0011

(b) Draw IAS (Von Neumann) Architecture and explain function of registers in it. [8]

Q.3 (a) State design factors in design of Instruction format. Draw instruction format for INTEL processor and explain various fields in it. [8]

(b) Draw and explain Programmer's model of 8086 [8]

OR

Q.4 (a) Draw timing Diagram for memory read Cycle of 8086 in Minimum Mode and List operations in each T state

(b) State and explain any 4 addressing modes with examples for 8086 processor. [8]

Q.5 (a) Draw and explain single bus organization of the CPU, showing all the registers and Data paths.

(b) Explain design of multiplier control unit using any hardwired design method. [8]

OR

Q.6 (a) Draw and explain general block diagram of the microprogrammed control unit. [8]

(b) Compare horizontal and vertical microinstruction representation. [8]

SECTION-II

Q.7 (a) What is cache Coherence and discuss MESI protocol? [8]

(b)Explain how a memory address is mapped into cache memory address using set associative mapped cache. The main memory is 64K words. The cache memory has 2048 words with block size of 128 words. [8]

OR

Q.8 (a) What is Virtual memory? Explain address translation mechanism for converting virtual address into physical address with neat diagram. [8]

(b) Write short note on (any two) [8]

1) SRAM

2) EPROM

3) RAID

Q.9 (a) What is DMA? Explain DMA Operation with diagram. [8]

(b) Write short notes on keyboard and scanner. [8]

OR

Q.10 (a) Compare :

1) Memory mapped I/O and I/O mapped I/O. [8]

2) Programmed I/O and interrupt driven I/O.

(b) Explain the working principle of the following : [8]

1) Laser Printer.

2) Video displays.

Q.11 (a) Draw and explain loosely coupled multiprocessor configuration with its merits. [10]

(b) Explain function level pipelining with diagram. [8]

OR

Q.12 Write Short note on (Any three): [18]

1) Super Scalar Architecture

2) RISC

3) Cluster

4) UMA

5) NUMA