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Total No. of Questions—12] [Total No. of Printed Pages—4

[3762]-231

S.E. (Information Technology) (I Semester) EXAMINATION, 2010

COMPUTER ORGANIZATION

(2008 COURSE)

Time : Three Hours **Maximum Marks : 100**

N.B. :— (*i*) Answer question No. **1** or **2**, **3** or **4**, and **5** or **6** from Section-I and question No. **7** or **8**, **9** or **10**, and **11** or **12** from Section-II.

(*ii*) Answers to the two Sections should be written in separate answer-books.

(*iii*) Neat diagrams must be drawn wherever necessary.

(*iv*) Figures to the right indicate full marks.

(*v*) Assume suitable data if necessary.

SECTION I

1. (*a*) Compare restoring and non-restoring division algorithm. Perform the division using restoring division Algorithm.

Dividend = 1000, Divisor = 11 [12]

(*b*) Draw IEEE standard single precision and double precision floating point formats and state various fields in it with their size and significance. [6]

P.T.O.

Or

2. (*a*) Draw flowchart of Booth's algorithm for signed multiplication and multiply the following signed 2's complement numbers. Justify your answer. [12]

Multiplicand = 11011 Multiplier = 00111

(*b*) Explain IAS (Von Neumann) architecture with the help of a neat diagram. [6]

3. (*a*) Explain with examples the following addressing modes of 8086 : [8]

(*i*) Index addressing

(*ii*) Register Indirect

(*iii*) Base index with displacement addressing

(*iv*) Auto Increment.

(*b*) Draw and explain programmer's model of 8086. [8]

Or

4. (*a*) Draw timing diagram for momory write cycle of 8086 and list operations in each T state. [8]

(*b*) Write a note on MAX/MIN mode of 8086. [8]

5. (*a*) Write a control sequence for execution of the instruction : Add (R_3), R1. [8]

(*b*) Draw and explain single bus organization of the CPU, showing all the registers and data paths. [8]

Or

6. (*a*) Compare horizontal and vertical microinstruction representation. [8]

(*b*) Explain the design of multiplier control unit using Delay Element Method. [8]

SECTION II

7. (*a*) Explain direct mapping technique with example. [10]

(*b*) A direct mapped cache has the following parameters :

Cache size = 1K words, Block size = 128 words and main memory size is 64K words. Specify the number of bits in TAG, BLOCK and WORD in main memory address. [8]

Or

8. (*a*) What is cache coherence and MESI protocol ? [10]

(*b*) Write short notes on (any *two*) : [8]

(*i*) EEPROM

(*ii*) RAID

(*iii*) SDRAM

(*iv*) DVD

9. (*a*) Write short notes on : [8]

(*i*) Keyboard

(*ii*) Scanner.

(*b*) Explain techniques for performing I/O. [8]

Or

10. (*a*) Explain DMA with neat diagram. [8]

(*b*) Explain functions and features of 8255 and 8251. [8]

11. (*a*) Compare closely coupled and loosely coupled multiprocessor configurations. Explain loosely coupled multiprocessor configuration. [10]

(*b*) Explain function level pipelining with diagram. [6]

Or

12. Write short notes on (any *four*) : [16]

(*i*) NUMA

(*ii*) UMA

(*iii*) RISC

(*iv*) CISC

(*v*) Cluster

(*vi*) Super Scalar Architecture