Nov- Dec - 2011

Total No. of Questions—**12**] [Total No. of Printed Pages—**4**

[4062]-211

S.E. (Information Technology) (I Sem.) EXAMINATION, 2011

COMPUTER ORGANIZATION

(2008 PATTERN)

Time : Three Hours **Maximum Marks : 100**

N.B. :— (*i*) Answer Question No. **1** *or* **2**, **3** *or* **4** and **5** *or* **6** from Section I and Question No. **7** *or* **8**, **9** *or* **10** and **11** *or* **12** from Section II.

(*ii*) Answers to the two Sections should be written in separate answer-books.

(*iii*) Neat diagrams must be drawn wherever necessary.

(*iv*) Figures to the right indicate full marks.

(*v*) Assume suitable data, if necessary.

SECTION I

1. (*a*) Draw flowchart of Booth's algorithm for signed multiplication. How bit pair recoding technique achieves faster multiplication. Bit pair recode multipliers $(110110101111001)_2$ and $(0101101010010101)_2$. [10]

(*b*) Draw IEEE standard single precision and double precision floating point formats. Represent – $(99.75)_{10}$ in single precision and double precision IEEE format. [8]

P.T.O.

Or

2. (*a*) Draw flowchart of Booth's algorithm for non-restoring unsigned division and divide the following unsigned numbers and justify your answer.

Dividend = $(15)_{10}$, Divisor = $(2)_{10}$. [10]

(*b*) Draw detailed Von Neumann architecture and explain function of registers in it. [8]

3. (*a*) Specify factors which decide instruction length. Draw and explain instruction format for INTEL processors. [8]

(*b*) Draw and explain functional block diagram of 8086. [8]

Or

4. (*a*) State addressing modes for the following instructions and show physical address generation : [8]

(*i*) MOV AX, [BX] [SI]

(*ii*) MOV CX, [DI]

(*iii*) MOV DX, [1234]

(*iv*) MOV BX, [BP] [DI] [0045]

(*b*) Draw timing diagram for memory cycle of 8086 and list operations in each T state. [8]

5. (*a*) Explain design of multiplier control unit using any hardwired design method. [8]

(*b*) For a single bus organization of CPU, write micro-operations and control signals for unconditional branch instruction. [8]

Or

6. (*a*) Draw and explain general block diagram of the microprogrammed control unit. [8]

(*b*) Compare : [8]

(*i*) Hardwired and microprogrammed control

(*ii*) Horizontal and vertical microinstruction format.

SECTION II

7. (*a*) Discuss set associative and fully associative cache mapping techniques with respect to mapping function, address structure, merits and demerits. [10]

(*b*) Discuss page replacement strategies in detail. [8]

Or

8. (*a*) What is virtual memory ? Explain address translation mechanism for converting virtual address into physical address with neat diagram. [10]

(*b*) Write short notes on (any *two*) : [8]

(*i*) EEPROM

(*ii*) SRAM

(*iii*) Optical disk

(*iv*) RAID.

9. (*a*) What is DMA ? Explain DMA operation with a diagram. Also explain data transfer modes in DMA. [8]

(*b*) Compare : [8]

(*i*) Programmed I/O and Interrupt driven I/O

(*ii*) Memory mapped I/O and I/O mapped I/O.

Or

10. (*a*) Explain the working principle of the following : [8]

(*i*) Laser printer

(*ii*) Keyboard.

(*b*) Compare : [8]

(*i*) Parallel and serial communication

(*ii*) Synchronous and asynchronous serial communication.

11. (*a*) Draw and explain loosely coupled multiprocessor configuration with its merits. [8]

(*b*) Explain briefly : [8]

(*i*) Instruction pipelining

(*ii*) Superscalar architecture.

Or

12. (*a*) What is cluster ? State advantages of clustering. Explain cluster classification. [8]

(*b*) Compare : [8]

(*i*) UMA & NUMA

(*ii*) RISC & CISC.